UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/538,576	06/15/2005	Marko Van Houdt	NL021302	9022

65913 7590 03/24/2008

NXP, B.V.
NXP INTELLECTUAL PROPERTY DEPARTMENT
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
PERILLA, JASON M	

ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
03/24/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/538,576	VAN HOUDT ET AL.	
	Examiner	Art Unit	
	JASON M. PERILLA	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-15 are pending in the instant application.

Information Disclosure Statement

2. The information disclosure statements (IDS) submitted on June 15, 2005 and May 30, 2006 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. § 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 7 and 14 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 7, one is unable to determine how said first clock means is to be "blocked" by said control signal. The meaning of "blocking" the first clock means can not be definitely determined because one is unable to determine how "blocking" modifies the function of the first clock means. For instance, one is unable to determine if "blocking" modifies an input to the clock means, an output of the clock means, or an internal function of the clock means. For purposes of applying prior art against the claim, "blocking" the first clock means is considered to modify the output of the first clock means.

Regarding claim 14, the claim is rejected for the same reasons as applied to claim 7 above.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-14 are rejected under 35 U.S.C. § 102(b) as being clearly anticipated by Buckland (U.S. Pat. No. 4744081).

Regarding claim 1, Buckland discloses a frame synchronizing (abstract) device for a binary data transmission system wherein digital data are transmitted as a serial bit stream (fig. 1, ref. 24) organized into frames (col. 1, lines 5-15; see also fig. 3), each frame including a pre-defined frameheader (i.e. "frame word"; col. 1, lines 20-25), comprising: a serial input (fig. 1, ref. 24) parallel output (fig. 1, "m") shift register means (fig. 1, refs. 16 and 18) for receiving said serial bit stream (fig. 1, "SERIAL DATA") and outputting said frames in a consecutive order, said shift register means (fig. 1, refs. 16 and 18) including a serial input portion (fig. 1, ref. 16) and a parallel output portion (fig. 1, "m", ref. 18) and having at least m stages ("m-bit words"; col. 2, line 65) as the number of bits in a frame (see discussion below), characterized by controlling means (*inter alia*, fig. 1, refs. 20, 22, 14, and 12) for detecting (fig. 1, ref. 14) whether or not a frameheader or "frame word" (fig. 1, "FRAME WORD") is present at the output of said parallel output portion and, if not, controlling (fig. 1, ref. 10; "SLIP") said shift register means so that the outputting of a frame from said parallel output portion is delayed by at least one time period which is needed for shifting a bit in said serial input portion from a

stage to a next one (col. 3, lines 20-40), until synchronization is reached (col. 2, lines 10-20). Buckland discloses that the serial input / parallel output shift register is the length of m-bits (fig. 1, ref. 16; col. 2, line 65). As broadly as claimed, each of Buckland's 8 bit search positions (see fig. 3) is considered to be a "frame". Therefore, the shift register has "at least as many stages as the number of bits of a frame" because it contains m bits (m is disclosed as 8 bits; col. 2, line 27) and m bits constitutes the length of a frame. As is conventionally understood, Buckland's 512 x 8 bits is considered a superframe.

Regarding claim 2, Buckland discloses the limitations of claim 1 as applied above. Further, Buckland discloses that said controlling means is adapted so that the delay of the outputting of a frame is repeated several times until synchronization is reached (col. 2, lines 10-20).

Regarding claim 3, Buckland discloses the limitations of claim 1 as applied above. Further, Buckland discloses that the frames have a fixed length of 8 bits as applied in claim 1 above.

Regarding claim 4, Buckland discloses the limitations of claim 1 as applied above. Further, Buckland discloses that the frames are bytes (i.e. 8 bits each) as applied to claim 1 above.

Regarding claim 5, Buckland discloses the limitations of claim 1 as applied above. Further, Buckland discloses a first clock means (fig. 1, ref. 20) for generating first clock pulses (fig. 1, "CLOCK") clocking said parallel output portion (fig. 1, ref. 18) of said shift register means (fig. 1, refs. 16 and 18), wherein controlling means are adapted

to control (via "SLIP" control; fig. 1) said first clock means so that said first clock pulses are delayed by at least one time period which is needed for shifting a bit in said serial input portion from a stage to a next one (col. 3, lines 20-40).

Regarding claim 6, Buckland discloses the limitations of claim 5 as applied above. Further, Buckland discloses that each frame (including the frame word) includes N or m bits (i.e. "N" = "m"; fig. 1; col. 37-39), a second clock means (not shown) is provided for generating second clock pulses (fig. 1, ref. 25) for clocking said serial input portion of said shift register means, and said first clock means (fig. 1, ref. 20) converts said second clock pulses into said first clock pulses (fig. 1, "CLOCK") having a time period which is N or m times (i.e. "N" – "m"; fig. 1, ref. 20, (÷ m DIVIDER") longer than the time period of said second clock pulses, characterized in that said controlling means is adapted to control said first clock means so that said first clock pulses are delayed by at least one time period of said second clock pulses (col. 3, lines 20-40).

Regarding claim 7, Buckland discloses the limitations of claim 5 as applied above. Further, Buckland discloses that said controlling means is adapted to supply a ("kick-pin") control signal (fig. 1, output of control circuit 10; "SLIP") to said first clock means (fig. 1, ref. 20), and said first clock means is adapted so that its output is modified by said control signal for at least one time period which is needed for shifting a bit in said serial input portion of said shift register means from a stage to a next one (col. 3, lines 20-40).

Regarding claim 8, Buckland discloses the limitations of the claim as applied to claim 1 above.

Regarding claim 9, Buckland discloses the limitations of claim 8 as applied above. Further, Buckland discloses the remaining limitations of the claim as applied to claim 2 above.

Regarding claim 10, Buckland discloses the limitations of claim 8 as applied above. Further, Buckland discloses the remaining limitations of the claim as applied to claim 3 above.

Regarding claim 11, Buckland discloses the limitations of claim 10 as applied above. Further, Buckland discloses the remaining limitations of the claim as applied to claim 4 above.

Regarding claim 12, Buckland discloses the limitations of claim 8 as applied above. Further, Buckland discloses the remaining limitations of the claim as applied to claim 5 above.

Regarding claim 13, Buckland discloses the limitations of claim 12 as applied above. Further, Buckland discloses the remaining limitations of the claim as applied to claim 5 above.

Regarding claim 14, Buckland discloses the limitations of claim 12 as applied above. Further, Buckland discloses the remaining limitations of the claim as applied to claim 5 above.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 15 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Buckland in view of Giorgetta et al (U.S. Pat. No. 7035292; "Giorgetta").

Regarding claim 15, Buckland discloses the limitations of claim 1 as applied above. Further, Buckland discloses that serial data is transported over a single channel (fig. 1, ref. 24) and, at the receiving side, is converted into parallel data (fig. 1, "m") for further processing. Buckland does not disclose the use of the device in a digital data transmission systems like SONET/SDH or Gigabit Ethernet. However, systems like SONET/SDH or Gigabit Ethernet are well known in the art as suggested by Giorgetta (col. 3, lines 20-30). Further, Giorgetta discloses synchronizing to a frame (col. 7, lines 1-30). In view of the disclosure of Giorgetta, one skilled in the art would have recognized that the exemplary frame synchronization device of Buckland is capable of frame synchronization in SONET and Gigabit Ethernet applications. Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made that the device of Buckland could be applied as a frame synchronization device in a SONET or Gigabit Ethernet application as suggested by Giorgetta because such applications require frame synchronization and are well known in the art.

9. Claims 1, 2, 5, 7-9, 12, and 14 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Surie (U.S. Pat. No. 4675886; cited in 6/15/05 IDS) in view of O'Connor et al (U.S. Pat. No. 5005191; "O'Connor").

Regarding claim 1, Surie discloses a frame synchronizing (abstract) device for a binary data transmission system wherein digital data are transmitted as a serial bit

stream (fig. 1, ref. 1) organized into frames (col. 1, lines 5-15), each frame including a pre-defined frameheader (i.e. "alignment word"), comprising: a serial input (fig. 1, ref. 1) parallel output shift register means (fig. 1, ref. 11) for receiving said serial bit stream and outputting said frames in a consecutive order, said shift register means including a serial input portion (fig. 1, ref. 11 "D") and a parallel output portion (fig. 1, ref. 11 "Q1-Q8") and having at least as many stages as the number of bits of the pre-defined frameheader (i.e. "alignment word" or "pattern"; col. 1, lines 65-68, col. 2, lines 29-33), characterized by controlling means (*inter alia*, fig. 1, refs. 13, 145, 143, and 12) for detecting whether or not a frameheader or alignment word is present at the output of said parallel output portion and, if not, controlling (fig. 1, ref. 12) said shift register means so that the outputting of a frame from said parallel output portion is delayed by at least one time period which is needed for shifting a bit in said serial input portion from a stage to a next one (col. 5, lines 53-63), until synchronization is reached (col. 5, lines 60-63). Surie discloses a frame synchronization device which permits frame synchronization and "significantly reduces the amount of data stored" (col. 2, lines 10-15). This is accomplished by determining the position of a frameheader or "alignment word" using a serial input / parallel output shift register (fig. 1, ref. 11) in an iterative shifting method to match a frameheader in the register with a known version of itself (i.e. the "completed pattern"; col. 2, lines 10-15). If the current phase position of the register does not contain the frameheader, the register is clocked with a phase shifting clock to alter the phase of the bit positions within the register by one (col. 2, lines 30-35; col. 5, lines 55-65). Surie discloses that the serial input / parallel output shift register is the

length of the frameheader or (col. 1, lines 65-68) which is "shorter relative to the duration of a frame by at least an order of magnitude" (col. 2, lines 10-15). Surie does not disclose that the register has "at least as many stages as the number of bits of a frame". However, O'Connor teaches, in strictly analogous art, synchronizing to a frame alignment using a serial input / parallel output shift register (fig. 3, ref. 12) having at least as many stages (i.e. fig. 3, "D0" - "D15") as the number of bits of a frame (fig. 3, "15 FRAME SHIFT REGISTER"). Specifically, O'Connor's register contains 15 frames of stages. O'Connor teaches that, using a register having more bit positions than the number of bits in a frame permits parallelism in the detection of a frame alignment word (col. 4, lines 10-20). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made that Surie's serial input / parallel output shift register could be replaced by one having more bit positions than contained in a frame to permit parallelism in the detection of a frame aligning frameheader as taught by O'Connor or as readily understood by one having ordinary skill in the art because it could lead to faster synchronization.

Regarding claim 2, Surie in view of O'Connor disclose the limitations of claim 1 as applied above. Further, Surie discloses that said controlling means is adapted so that the delay of the outputting of a frame is repeated several times until synchronization is reached (col. 5, lines 55-65).

Regarding claim 5, Surie in view of O'Connor disclose the limitations of claim 1 as applied above. Further, Surie discloses a first clock means (fig. 1, ref. 12) for generating first clock pulses clocking said parallel output portion (fig. 1, ref. 11, "CP") of

said shift register means (fig. 1, ref. 11), wherein controlling means are adapted to control said first clock means so that said first clock pulses are delayed (i.e. "moved back:") by at least one time period which is needed for shifting a bit in said serial input portion from a stage to a next one (col. 5, lines 50-65).

Regarding claim 7, Surie in view of O'Connor disclose the limitations of claim 5 as applied above. Further, Surie discloses that said controlling means is adapted to supply a ("kick-pin") control signal (fig. 1, output of register 143) to said first clock means (fig. 1, ref. 12), and said first clock means is adapted so that its output is modified by said control signal for at least one time period which is needed for shifting a bit in said serial input portion of said shift register means from a stage to a next one (col. 5, lines 50-65).

Regarding claim 8, Surie in view of O'Connor disclose the limitations of the claim as applied to claim 1 above.

Regarding claim 9, Surie in view of O'Connor disclose the limitations of claim 8 as applied above. Further, Surie discloses the remaining limitations of the claim as applied to claim 2 above.

Regarding claim 12, Surie in view of O'Connor disclose the limitations of claim 8 as applied above. Further, Surie discloses the remaining limitations of the claim as applied to claim 5 above.

Regarding claim 14, Surie in view of O'Connor disclose the limitations of claim 12 as applied above. Further, Surie discloses the remaining limitations of the claim as applied to claim 7 above.

10. Claims 3, 4, 10, and 11 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Surie in view of O'Connor and Bruekheimer (U.S. Pat. No. 5367544).

Regarding claim 3, Surie in view of O'Connor disclose the limitations of claim 1 as applied above. Surie in view of O'Connor do not explicitly disclose that the frames have a fixed length. However, using a fixed length frame is notoriously known in the art as evidenced by Bruekheimer (col. 2, lines 5-15) in strictly analogous art (abstract). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made that the frame synchronizing device of Surie in view of O'Connor could be utilized with a fixed frame length as noted by Bruekheimer because the use of fixed frame lengths is well known and accepted in the art.

Regarding claim 4, Surie in view of O'Connor and Bruekheimer disclose the limitations of claim 3 as applied above. Further, it would have been obvious to one having ordinary skill in the art at the time which the invention was made that the length of a frame in the combination of Surie in view of O'Connor and Bruekheimer could be 8 bits or one byte. Alternatively, it would have been obvious to utilize any number of bits in a frame because the number of bits in a frame is a simple design choice. Moreover, the use of 8 bits per frame is not described in the specification as applying to any particular advantage or feature in the present invention over the conventional art.

Regarding claim 10, Surie in view of O'Connor disclose the limitations of claim 8 as applied above. Further, Surie in view of O'Connor and Bruekheimer disclose the remaining limitations of the claim as applied to claim 3 above.

Regarding claim 11, Surie in view of O'Connor disclose the limitations of claim 8 as applied above. Further, Surie in view of O'Connor and Bruekheimer disclose the remaining limitations of the claim as applied to claim 4 above.

11. Claim 15 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Surie in view of O'Connor and Giorgetta.

Regarding claim 15, Surie in view of O'Connor disclose the limitations of claim 1 as applied above. Further, Surie discloses that serial data is transported over a single channel (fig. 1, ref. 11) and, at the receiving side, is converted into parallel data (col. 1, lines 20-25; col. 1, lines 65-66) for further processing. Surie in view of O'Connor do not disclose the use of the device in a digital data transmission systems like SONET/SDH or Gigabit Ethernet. However, systems like SONET/SDH or Gigabit Ethernet are well known in the art as suggested by Giorgetta (col. 3, lines 20-30). Further, Giorgetta discloses synchronizing to a frame (col. 7, lines 1-30). In view of the disclosure of Giorgetta, one skilled in the art would have recognized that the exemplary frame synchronization device of Surie in view of O'Connor is capable of frame synchronization in SONET and Gigabit Ethernet applications. Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made that the device of Surie in view of O'Connor could be applied as a frame synchronization device in a SONET or Gigabit Ethernet application as suggested by Giorgetta because such applications require frame synchronization and are well known in the art.

Conclusion

12. The prior art of record not relied upon above but cited on the accompanying PTO-892 form is presented by the Examiner to further show the state in the art with respect to carrier frequency recovery.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JASON M. PERILLA whose telephone number is (571)272-3055. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jason M Perilla/
Primary Examiner, Art Unit 2611
March 18, 2008

jmp